

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): David Christopher Burden

Confirmation No.:

Application No.:

Examiner:

Filing Date: Herewith

Group Art Unit:

Title: CHARGE RATIONING AWARE SCHEDULER

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

- ☒ under 37 CFR 1.97(b), or
(Within three months of filing national application; or date of entry of national application; or before mailing date of first office action on the merits; whichever occurs last)
- ☐ under 37 CFR 1.97(c) together with either a:
☐ Statement under 37 CFR 1.97(e), or
☐ a \$180.00 fee under 37 CFR 1.17(p), or
(After the 37 CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs first)
- ☐ under 37 CFR 1.97 (d) together with a:
☐ Statement under 37 CFR 1.97(e)(1) or (2), and
☐ a \$180.00 fee set forth in 37 CFR 1.17(p).
(Filed after final action, a notice of allowance, on or before payment of the issue fee)

Please charge to Deposit Account **08-2025** the sum of \$0.00. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **08-2025** pursuant to 37 CFR 1.25.

☒ Applicant(s) submit herewith Form PTO 1449 - Information Disclosure Statement together with any required copies of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

☐ A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individual(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO 1449 and is enclosed herewith.

It is requested that the information disclosed herein be made of record in this application.

"Express Mail" label no. **EL987550785US**

Date of Deposit **11/03/03**

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Commissioner for Patents, Alexandria, VA 22313-1450.

By

Doreen Melchior

Typed Name: Doreen Melchior

Respectfully submitted,

David Christopher Burden

By

Peter Kraguljac
Peter Kraguljac

Attorney/Agent for Applicant(s)
Reg. No. **38,520**

Date: **11/03/03**

PATENT APPLICATION

Sheet 1 of 1

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. 200309887-1	APPLICATION NO.	CONFIRMATION NO.
APPLICANT David Christopher Burden			
FILING DATE Herewith		GROUP	

REFERENCE DESIGNATION U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	1A	2003/0028816	02/06/2003	Bacon	
	1B				
	1C				
	1D				
	1E				
	1F				
	1G				
	1H				
	1I				
	1J				
	1K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L					
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	1Q	On-Line Scheduling of Hard Real-Time Tasks on Variable Voltage Processor; Inki Hong, Miodrag Potkonjak and Mani B. Srivastava; Computer Science Dept., Univ. of CA, LA, CA; and Electrical Engineering Dept., Univ. of CA, LA, CA
	1R	PASA: A Software Architecture For Building Power Aware Embedded Systems; Cristiano Pereira and Rajesh Gupta; Dept. of Information and Computer Science, University of California, Irvine; and Mani Srivastava; Dept. of Electrical Engineering, University of CA, Los Angeles
	1S	A Power-Aware, Best-Effort Real-Time Task Scheduling Algorithm; Jिंगgang Wang, Binoy Ravindran, and Tom Martin; The Bradley Dept. of Electrical and Computer Engineering, Virginia Tech, Blacksburg, VA

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	1L					
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	1Q	20.4 A 0.9V to 1.95V Dynamic Voltage-Scalable and Frequency-Scalable 32b PowerPC Processor; Nowka, Carpenter, MacDonald, Ngo, Brock, Ishii, Nguyen & Burns; IBM Austin Research Lab; IBM Microelectronics Division, Austin, TX; IBM Microelectronics Div., Yasu, Japan; ISSCC 2002 / Session 20 / Microprocessors / 20.4; 2002 IEEE International Solid-State Circuits Conference; 0-7803-7335-9
	1R	Power-Aware Scheduling for Embedded Systems under Min/Max Power and Timing Constraints; Liu, Chou, & Bagherzadeh; Dept. of Electrical & Computer Engineering; University of California, Irvine; and Aranki, & Toomarian; California Institute of Technology; Jet Propulsion Laboratory, Pasadena, CA
	1S	Energy Aware Scheduling for Distributed Real-Time Systems; Misshra, Rastogi, Zhu, Mosse & Melhem; Computer Science Dept., University of Pittsburgh, Pittsburgh, PA

EXAMINER

DATE CONSIDERED